What is claimed is:

1. A pipeline analog-to-digital converter for obtaining a digital output signal of a predetermined bits, corresponding to an analog input signal as the target for conversion, by executing pipeline processing based on a clock signal, said pipeline analog-to-digital converter comprising a plurality of analog-to-digital conversion stages connected in series, each comprising:

a sub-A / D converter for converting an analog input voltage into a digital signal of 1.5 bits;

a sub-D / A converter for converting the digital signal into an analog voltage; and

an amplifier for sampling and holding a difference in voltage between the input voltage and the analog voltage and amplifying the difference in voltage as held, wherein the analog-to-digital conversion stage to which the analog input signal is delivered, in the initial stage of said plurality of the analog-to-digital conversion stages, comprises a first amplifier for sampling and holding the analog input signal to thereby output a voltage equivalent to 1 / N of the analog input signal as a first analog voltage, a first sub-A / D converter for converting the first analog voltage into a first digital signal of 1.5 bits, a first sub-D / A converter for converting the first digital signal into a second analog voltage, a second amplifier for sampling and holding a difference in voltage between the first and second

analog voltages, and amplifying the difference in voltage as held by a factor of N to thereby output a third analog voltage, a second sub-A / D converter for converting the third analog voltage into a second digital signal of 1.5 bits, a second sub-D / A converter for converting the second digital signal into a fourth analog voltage, a third amplifier for sampling and holding a difference in voltage between the third and fourth analog voltages, and amplifying the difference in voltage as held by a factor of two to be thereby delivered to the analog-to-digital conversion stage in the next stage, and a discriminator for generating a digital signal of 1.5 bits, corresponding to the most significant bit, on the basis of the first and second digital signals.

2. A pipeline analog-to-digital converter according to claim 1, wherein N is a value selected from numerical values consisting of two and four.

3. A pipeline analog-to-digital converter for obtaining a digital output signal of a predetermined bits, corresponding to an analog input signal as the target for conversion, by executing pipeline processing based on a clock signal, said pipeline analog-to-digital converter comprising a plurality of analog-to-digital conversion stages connected in series, each comprising:

a sub-A / D converter for converting an analog input voltage into a digital signal of 1.5 bits;

a sub-D / A converter for converting the digital signal into an analog

voltage; and

an amplifier for sampling and holding a difference in voltage between the input voltage and the analog voltage and amplifying the difference in voltage as held, wherein the analog-to-digital conversion stage to which the analog input signal is delivered, in the initial stage of said plurality of the analog-to-digital conversion stages, comprises a first holder for holding and outputting a voltage obtained by adding a reference voltage to the analog input signal, a second holder for holding and outputting the analog input signal, a third holder for holding and outputting a voltage obtained by subtracting the reference voltage from the analog input signal, a first sub-A/ D converter for comparing the analog input signal with a voltage equivalent to ± 1 / 2 of the reference voltage to thereby convert the analog input signal into a first digital signal of 1.5 bits, selectors for selecting a voltage outputted from any one of the first, the second, and the third holder, in accordance with the first digital signal, to thereby output as a first analog voltage, a second sub-A / D converter for converting the first analog voltage into a second digital signal of 1.5 bits, a sub-D / A converter for converting the second digital signal into a second analog voltage, an amplifier for sampling and holding a difference in voltage between the first and second analog voltages, and amplifying the difference in voltage as held by a factor of two so as to be delivered to the analog-to-digital conversion stage in the next stage, and a discriminator for generating a digital signal of 1.5 bits,

corresponding to the most significant bit, on the basis of the first and second digital signals.